



# UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE  
United States Patent and Trademark Office  
Address: COMMISSIONER FOR PATENTS  
P.O. Box 1450  
Alexandria, Virginia 22313-1450  
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/648,054	08/26/2003	Matthew Russell	03-0154	2925
24319	7590	05/19/2005	EXAMINER ANDUJAR, LEONARDO	
LSI LOGIC CORPORATION 1621 BARBER LANE MS: D-106 MILPITAS, CA 95035			ART UNIT 2826	

DATE MAILED: 05/19/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

**Office Action Summary**

Application No.

10/648,054

Applicant(s)

RUSSELL ET AL.

Examiner

Leonardo Andújar

Art Unit

2826

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 22 March 2005.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-11 is/are pending in the application.
- 4a) Of the above claim(s) 9-11 is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-8 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date 08/03
- 4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_\_
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: \_\_\_\_\_

## **DETAILED ACTION**

### ***Election/Restrictions***

1. Applicant's election with traverse of Group I (claims 1-8) in a communication filed on 03/22/2005 is acknowledged. The traversal is on the ground(s) that the subject matter of claims 1-11 is sufficiently related that a thorough and complete search for the subject matter of the elected claims would necessarily encompass a thorough and complete search for the subject matter of the non-elected claims. This is not found persuasive because referring to the restriction requirement set forth in the election requirement, it clearly shows that the alternative method proposed by the examiner would be distinct from the process claimed. Additionally, the search is not coextensive as evidenced by the different fields of search for the process and product as cited in the previous restriction requirement. Furthermore, Applicant has not provided a convincing argument that the materially different processes would not be suitable in producing the claimed device. Note that the unpatentability of the Group I invention would not necessarily imply unpatentability of the Group II invention. Thus the requirement is still deemed proper and is therefore made FINAL.

### ***Claim Rejections - 35 USC § 102***

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

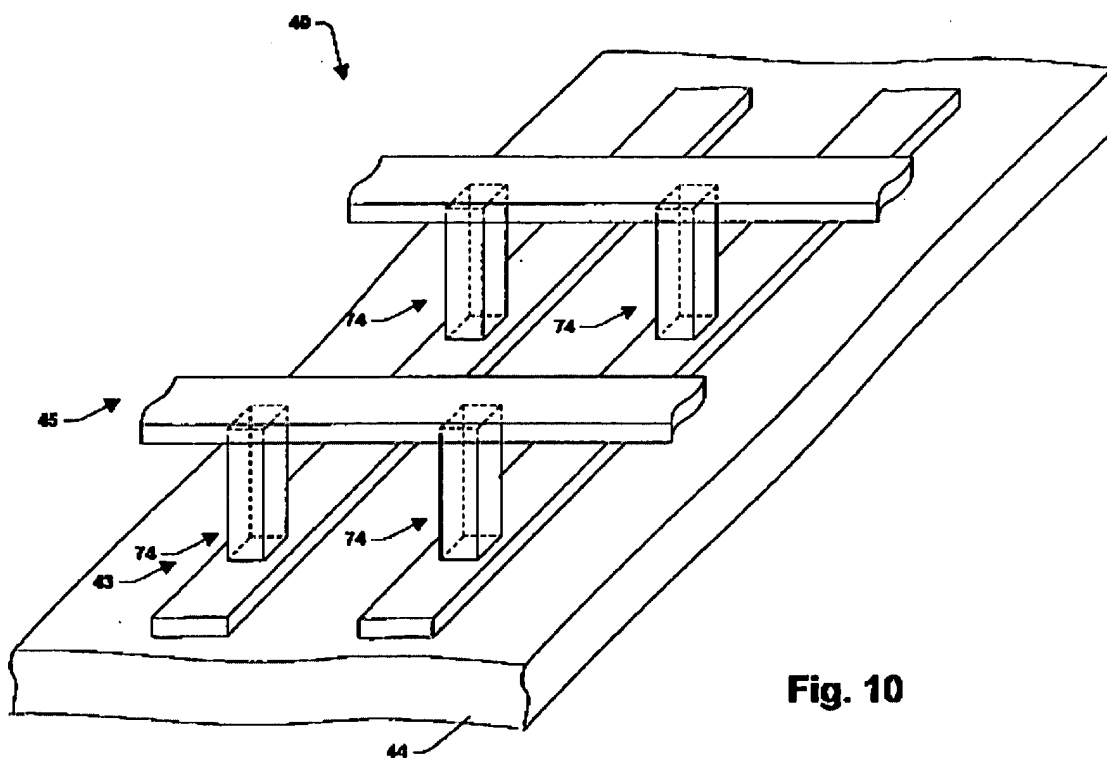
A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Art Unit: 2826

3. Claims 1-8 are rejected under 35 U.S.C. 102(b) as being anticipated by Nogami et al. (US 6,060,383).

4. Regarding claim 1, Nogami (e.g. figs. 10 and 15) shows a bus layout design comprising: a first electrically conductive layer 45 including at least a first bus and a second bus, a second electrically conductive layer 43 including at least a first bus and a second bus, an electrically insulating layer disposed between the first electrically conductive layer and the second electrically conductive layer, a plurality of vias 75 (see fig. 5; i.e. 70) through the electrically insulating layer 54 conductively connecting the first electrically conductive layer and the second electrically conductive layer and arranged such that the first bus and the second bus of the first electrically conductive layer are electrically connected.



**Fig. 10**

5. Regarding claim 2, Nogami shows that the plurality of vias connecting the first electrically conductive layer and the second electrically conductive layer are arranged such that the first bus and the second bus of the second electrically conductive layer are electrically connected

6. Regarding claim 3, Nogami shows that the first and second bus of the first electrically conductive layer overlap the second bus of the second electrically conductive layer.

7. Regarding claim 4, Nogami shows that the first and second buses of the first electrically conductive layer overlap the first and second buses of the second electrically conductive layer across the entire input/output width.

8. Regarding claim 5, Nogami shows that the plurality of vias connecting the first electrically conductive layer and the second electrically conductive layer are arranged such that the first bus and the second bus of the second electrically conductive layer are electrically connected; and wherein the first and second bus of the first electrically conductive layer overlaps the first and second bus of the electrically conductive layer; across the entire input/output width.

9. Regarding claim 6, Nogami (e.g. figs. 10 and 15) a bus layout design comprising: a first electrically conductive layer 45 including a plurality of buses not conductively connected to each other on the first electrically conductive layer; a second electrically conductive layer 43 including a plurality of buses not conductively connected to each other on the second electrically conductive layer; an electrically insulating layer 45 disposed between the first electrically conductive layer and the second electrically conductive layer; and wherein at least one bus on the first electrically conductive layer is conductively connected to at least one bus on the second electrically conductive layer through the electrically insulating layer.

10. Regarding claim 7, Nogami shows at least one bus on the first electrically conductive layer overlaps with at least one bus on the second electrically conductive layer.

11. Regarding claim 8, Nogami shows a plurality of vias 75 (see fig. 5; i.e. 70) through the electrically insulating layer, the vias conductively connect at least one bus on the first electrically conductive layer to at least one bus on the second electrically conductive layer.

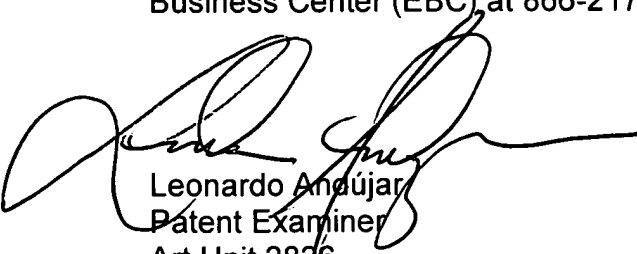
Art Unit: 2826

**Conclusion**

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Leonardo Andújar whose telephone number is 571-272-1912. The examiner can normally be reached on Mon through Thu from 9:00 AM to 7:30 PM EST.

13. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan J. Flynn can be reached on 571-272-1915. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

14. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Leonardo Andújar  
Patent Examiner  
Art Unit 2826  
05/10/2005